



COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 3201 P R No : 201108381 Sex : F Name : GOVEKAR DIVYA DIGAMBAR
No Of Attempts : 2

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA	Theory	4	BC +	
	IA	2	BC +	
Digital Signal Processors & Embedded Systems	Theory	4	CC +	
	IA	2	CC +	
Design for Testability & E-Waste Management	Theory	4	CC +	
	IA	2	BC +	
Processor Architecture & Parallel Processing	Theory	4	BB P	
	IA	2	CC +	
Memory Design	Theory	4	CC +	
	IA	2	BC +	
Parallel Processing Lab	IA	2	BC +	
	Practical	2	CC +	
FPGA & Embedded Systems Lab	IA	2	AB +	
	Practical	2	AB +	
Total :		38		5.84 P PASSES

Seat No : 3202 P R No : 201006308 Sex : F Name : NAIK STHRIGDHARA NAVANATH
No Of Attempts : 2

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA	Theory	4	BB +	
	IA	2	AA +	
Digital Signal Processors & Embedded Systems	Theory	4	BB +	
	IA	2	BB +	
Design for Testability & E-Waste Management	Theory	4	AB +	
	IA	2	BC +	
Processor Architecture & Parallel Processing	Theory	4	BB P	
	IA	2	BB +	
Memory Design	Theory	4	AA +	
	IA	2	AB +	
Parallel Processing Lab	IA	2	AB +	
	Practical	2	CC +	
FPGA & Embedded Systems Lab	IA	2	BB +	
	Practical	2	BB +	
Total :		38		7.37 P PASSES

2481
15/2/17

To
PPL
861
15/2/17

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RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION
HELD IN NOVEMBER 2016
Course : Revised Course - 2013

COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No: 3203 P R No: 200801358 Sex: F Name: PARKER NEHA PRASAD
No Of Attempts : 3

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA	Theory	4	AA +	
	IA	2	AA +	
Digital Signal Processors & Embedded Systems	Theory	4	BC +	
	IA	2	BB +	
Design for Testability & E-Waste Management	Theory	4	AB +	
	IA	2	AA +	
Processor Architecture & Parallel Processing	Theory	4	BC P	
	IA	2	BB +	
Memory Design	Theory	4	AA +	
	IA	2	AA +	
Parallel Processing Lab	IA	2	BC +	
	Practical	2	BC +	
FPGA & Embedded Systems Lab	IA	2	AB +	
	Practical	2	AB +	
Total :		38		7.63 P PASSES

Seat No: 3204 P R No: 201107719 Sex: M Name: PATIL ABHIJEET VILAS
No Of Attempts : 2

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA	Theory	4	BB +	
	IA	2	BB +	
Digital Signal Processors & Embedded Systems	Theory	4	BC +	
	IA	2	CC +	
Design for Testability & E-Waste Management	Theory	4	BC +	
	IA	2	BC +	
Processor Architecture & Parallel Processing	Theory	4	BB P	
	IA	2	BB +	
Memory Design	Theory	4	BC +	
	IA	2	BB +	
Parallel Processing Lab	IA	2	BB +	
	Practical	2	CC +	
FPGA & Embedded Systems Lab	IA	2	AB +	
	Practical	2	AB +	
Total :		38		6.53 P PASSES

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RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION
HELD IN NOVEMBER 2016
Course : Revised Course - 2013

COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 3205 P R No : 201007394 Sex : M Name : SHETGAONKAR ANAY ANIL
No Of Attempts : 2

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA	Theory	4	BC +	
	IA	2	BB +	
Digital Signal Processors & Embedded Systems	Theory	4	CC +	
	IA	2	CC +	
Design for Testability & E-Waste Management	Theory	4	BC P	
	IA	2	CC +	
Processor Architecture & Parallel Processing	Theory	4	BB P	
	IA	2	BC +	
Memory Design	Theory	4	CC +	
	IA	2	CC +	
Parallel Processing Lab	IA	2	BB +	
	Practical	2	BC +	
FPGA & Embedded Systems Lab	IA	2	CC +	
	Practical	2	BC +	
Total :		38	5.79 P PASSES	

Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
BB	7	Good
BC	6	Fair
CC	5	Satisfactory
FF	0	Fail

Read By : *pphate*
Checked By : *KM*

Date : 14/2/2017

S. J. Figueiredo
13/2/2017
S. J. Figueiredo
Assistant Registrar-E(Prof.)

Leo V. Macedo
13/2/17
Leo V. Macedo
Controller Of Examinations

Y. V. Reddy
14/2/17
Prof. Y. V. Reddy
Registrar



KM